AN OPERATING METHOD FOR DETECTING AND SOLVING UNDERFLOW AND OVERFLOW BY USING OVERSAMPLING

BACKGROUND OF THE INVENTION

Field of Invention

[0001] The present invention generally relates to an operating method for detecting and solving underflow and overflow. And more particularly, to an operating method for detecting and solving underflow and overflow by using oversampling.

Description of Related Art

[0002] When a transmitter and a receiver are using the same clock frequency to transmit and receive data, the bit number of the data received by the receiver is the same as the physical data. Thus, there is no underflow and overflow. However, when the transmitter and the receiver are using different clock frequencies to transmit and receive data, this leads to the generation of underflow and overflow. When the clock frequency of the receiver is higher than the clock frequency of the transmitter, the bit number of the data received is more than the bit number of the data transmitted by the transmitter. This phenomenon is known as underflow. When the clock frequency of the receiver is lower than the clock frequency of the transmitter, the bit number of the data received is less than the bit number of the data transmitted by the transmitter. This phenomenon is known as overflow. When the transmitter and the receiver operate in different clock frequencies, there is no adequate method for detecting and solving the underflow and the overflow problems in the prior art.

SUMMARY OF THE INVENTION

[0003] In order to solve the problems mentioned above, the present invention provides an operating method for detecting and solving underflow and overflow by using oversampling. When the clock frequency of the transmitter is different from the receiver, the present invention is able to detect and solve the underflow and the overflow problems that result from the different operation frequencies of the transmitter and the receiver.

[0004] To achieve the objective mentioned above, the present invention provides an operating method for detecting and solving underflow and overflow by using oversampling. The operating method is suitable for the transmitter and the receiver that use different clock frequencies to transmit data. Wherein, the receiver receives a plurality of received packages, each received package includes a plurality of data, each data is sampled by using a plurality of sampling phases, and the sampling phase that is located in the front edge of each data is referred to as the leading edge sampling phase. In the present operating method, at first, the leading edge sampling phase of each received package having the most frequency in the first synchronous period is used as the initial leading edge phase. Afterwards, the underflow circulation center point and overflow circulation center point are determined. Then, the underflow operation and the overflow operation are processed according to the underflow circulation center point and overflow circulation center point. The extra bit is thrown away when the underflow operation is processing, and the lost bit is inserted when the overflow operation is processing. Wherein, when these sampling phases have n (n is a positive odd number) sampling phases, the phase shift of the leading edge sampling phase that is located in between the (n+1)/2th sampling phase and the ([(n+1)/2]+1th sampling phase is used as the underflow circulation center point and overflow circulation center point. When these sampling

phases have m (m is a positive even number) sampling phases, the leading edge sampling phase that is located in the [(m/2)+1]th sampling phase is used as the underflow circulation center point and overflow circulation center point.

[0005] The present invention further provides an operating method for detecting and solving the underflow problem by using oversampling. The operating method is suitable for a transmitter and a receiver that are using different clock frequencies to transmit data. Wherein, the receiver receives a plurality of received packages, each received package includes a plurality of data, each data is sampled by using a plurality of sampling phases, and the sampling phase that is located in the front edge of each data is referred to as the leading edge sampling phase. In the operating method, at first, the leading edge sampling phase of each received package having the most frequency in the first synchronous period is used as the initial leading edge phase. Afterwards, the underflow circulation center point is determined. Then, the underflow operation is processed according to the underflow circulation center point. When the underflow operation is processing, the extra bit is thrown away. Wherein, when these sampling phases have n (n is a positive odd number) sampling phases, the phase shift of the leading edge sampling phase that is located in between the (n+1)/2th sampling phase and the ([(n+1)/2]+1th sampling phase is used as the underflow circulation center point. When these sampling phases have m (m is a positive even number) sampling phases, the leading edge sampling phase that is located in the [(m/2)+1]th sampling phase is used as the underflow circulation center point.

[0006] The present invention further provides an operating method for detecting and solving the overflow problem by using oversampling. The operating method is suitable for the transmitter and the receiver that are using different clock frequencies to transmit

data. Wherein, the receiver receives a plurality of received packages, each received package includes a plurality of data, each data is sampled by using a plurality of sampling phases, and the sampling phase that is located in the front edge of each data is referred to as the leading edge sampling phase. In the operating method, at first, the leading edge sampling phase of each received package having the most frequency in the first synchronous period is used as the initial leading edge phase. Afterwards, the overflow circulation center point is determined. Then, the overflow operation is processed according to the overflow circulation center point. When the overflow operation is processing, the lost bit is inserted. Wherein, when these sampling phases have n (n is a positive odd number) sampling phases, the phase shift of the leading edge sampling phase that is located in between the (n+1)/2th sampling phase and the ([(n+1)/2]+1th sampling phase is used as the overflow circulation center point. When these sampling phases have m (m is a positive even number) sampling phases, the leading edge sampling phase that is located in the [(m/2)+1]th sampling phase is used as the overflow circulation center point.

[0007] As all mentioned above, the present invention is capable of detecting the timing of the underflow and the overflow when the clock frequencies of the transmitter and the receiver are different. The present invention is also able to compensate properly when the underflow and the overflow happen, to ensure the bit number of the data received by the receiver is the same as the physical data. Thus, the underflow and the overflow problems are solved.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The

drawings illustrate embodiments of the invention, and together with the description, serve to explain the principles of the invention. In the drawings,

[0009] FIG. 1 is a phase shift diagram of the leading edge sampling phase of the oversampling using n (n is a positive odd number) sampling phases;

[0010] FIG. 2 is a phase shift diagram of the leading edge sampling phase of the oversampling using m (m is a positive even number) sampling phases;

[0011] FIG. 3 is an underflowed phase shift diagram of the leading edge sampling phase of an embodiment using the operating method that is capable of detecting and solving underflow and overflow by using oversampling according to the present invention;

[0012] FIG. 4 is an underflowed sampling phase diagram of an embodiment using the operating method that is capable of detecting and solving underflow and overflow by using oversampling according to the present invention;

[0013] FIG. 5 is an overflowed phase shift diagram of the leading edge sampling phase of an embodiment using the operating method that is capable of detecting and solving underflow and overflow by using oversampling according to the present invention; and

[0014] FIG. 6 is an overflowed sampling phase diagram of an embodiment using the operating method that is capable of detecting and solving underflow and overflow by using oversampling according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0015] Referring to FIG. 1, it schematically shows a phase shift diagram of the leading edge sampling phase of the oversampling using n (n is a positive odd number) sampling phases. As shown in FIG. 1, when the sampling phases have n (n is a positive odd number) sampling phases, the phase shift of the leading edge sampling phase that is located in

between the (n+1)/2th sampling phase and the ([(n+1)/2]+1th sampling phase is referred to as the underflow circulation center point and overflow circulation center point. FIG. 2 schematically shows a phase shift diagram of the leading edge sampling phase of the oversampling using m (m is a positive even number) sampling phases. When the sampling phases have m (m is a positive even number) sampling phases, the leading edge sampling phase that is located in the [(m/2)+1]th sampling phase is referred to as the underflow circulation center point and overflow circulation center point. Before the embodiment is described, it is worth to note that even oversampling of 5 sampling phases is exemplified for easy explanation, to those who are skilled in the art, and the oversampling of several sampling phases is also adapted to the present invention, as long as the oversampling has several sampling phases.

[0016] In the present embodiment, the transmitter and the receiver are operated in different clock frequencies, and each bit of the data received by the receiver is sampled by using the oversampling structure of the 5 sampling phases. The receiver receives a plurality of received packages when the transmitter sends the data, each received package includes a plurality of data, each data is sampled by using 5 sampling phases, and the sampling phase that is located in the front edge of each data is referred to as the leading edge sampling phase. Afterwards, the leading edge sampling phase of each received package having the most frequency in the first synchronous period is used as the initial leading edge phase. Furthermore, when each data is sampled, a sampling phase that is sampled from the leading edge sampling phase of each data is sampled. In the present embodiment, when each data is sampled, the second sampling phase after the leading edge sampling phase that is corresponding to each data is sampled.

[0017] Then, as shown in FIG. 1, when the leading edge sampling phase shifts between phase 3 and phase 4, referred to as the circulation center point, that is, when the leading edge sampling phase shifts between phase 3 and phase 4, the phase shift between phase 3 and phase 4 is used as the underflow circulation center point and the overflow circulation center point.

[0018] Referring to FIG. 3, it schematically shows an underflowed phase shift diagram of the leading edge sampling phase of an embodiment using the operating method that is capable of detecting and solving the underflow and the overflow by using the oversampling according to the present invention. In FIG. 3, each data received by the receiver is comprised of 5 sampling phases. These 5 sampling phases are phase 1 (30), phase 2 (32), phase 3 (34), phase 4 (36) and phase 5 (38). In the present embodiment, it is assumed that phase 1 (30) is the package initial phase. That is, phase 1 (30) is also the initial leading edge phase. Referring to FIG. 4, it schematically shows an underflowed sampling phase diagram of an embodiment using the operating method that is capable of detecting and solving underflow and overflow by using oversampling according to the present invention. As shown in FIG. 4, since the clock frequency of the receiver is higher than the clock frequency of the transmitter, the phase shift of the leading edge phase is shifted according to the sequence of phase 1 (30) to phase 2 (32), phase 3 (34), phase 4 (36), phase 5 (38), phase 1 (30). In FIG. 4, when the leading edge phase shifts from phase 3 (34) to phase 4 (36), since the bit number of the data received is more than 1 compared to the physical data, this leads to the underflow circumstance being generated, therefore a need exists for throwing away one extra bit, and this is referred to as the underflow operation. In the physical hardware circuit, an underflow signal may be enabled at this

time, which subsequently throws away one extra bit, so that the bit number of the data received by the receiver is the same as the physical data.

[0019] In addition, if the data received by the receiver includes a big noise or the clock frequency of the receiver is much higher than the clock frequency of the transmitter, the leading edge phase shifts 2 phases one time rather than the original 1 phase shift. Referring the FIG. 3 again, when the leading edge phase shifts from phase 2 (32) to phase 4 (36), or shifts from phase 3 (34) to phase 5 (38), it also results in the bit number of the received data being more than one bit compared to the physical data, and this leads to the underflow circumstance being generated, therefore a need exists for throwing away one extra bit, and this is referred to as the underflow operation. In the physical hardware circuit, an underflow signal may be enabled at this time, which subsequently throws away one extra bit, so that the bit number of the data received by the receiver is the same as the physical data. As described above, the present invention is able to detect the timing of the underflow and solve the underflow problem.

[0020] Referring to FIG. 5, it schematically shows an overflowed phase shift diagram of the leading edge sampling phase of an embodiment using the operating method that is capable of detecting and solving underflow and overflow by using oversampling according to the present invention. In FIG. 5, the data received by the receiver is comprised of 5 sampling phases. These 5 sampling phases are phase 1 (50), phase 2 (52), phase 3 (54), phase 4 (56) and phase 5 (58). In the present embodiment, it is assumed that the phase 1 (50) is the package initial phase. That is, phase 1 (50) is also the initial leading edge phase. Referring to FIG. 6, it schematically shows an overflowed sampling phase diagram of an embodiment using the operating method that is capable of detecting and solving the underflow and the overflow by using the oversampling according to the

present invention. As shown in FIG. 6, since the clock frequency of the receiver is lower than the clock frequency of the transmitter, the phase shift of the leading edge phase is shifted according to the sequence of the phase 1 (50), phase 5 (58), phase 4 (56), phase 3 (54), phase 2 (52), phase 1 (50). In FIG. 6, when the leading edge phase shifts from phase 4 (56) to phase 3 (54), since the bit number of the data received is less than 1 compared to the physical data, this leads to the overflow circumstance being generated, therefore a need exists for inserting one extra bit, and this is referred to as the overflow operation. In the physical hardware circuit, an overflow signal may be enabled at this time, which subsequently inserts one extra bit, so that the bit number of the data received by the receiver is the same as the physical data.

[0021] In addition, if the data received by the receiver includes a big noise or the clock frequency of the receiver is much lower than the clock frequency of the transmitter, the leading edge phase shifts 2 phases one time rather than the original 1 phase shift. Referring the FIG. 5 again, when the leading edge phase shifts from phase 4 (56) to phase 2 (52), or shifts from phase 5 (58) to phase 3 (54), it also results in the bit number of the received data being less than one bit compared to the physical data, this leads to the overflow circumstance being generated, therefore a need exists for inserting one extra bit, and this is referred to as the overflow operation. In the physical hardware circuit, an overflow signal may be enabled at this time, which subsequently inserts one extra bit, so that the bit number of the data received by the receiver is the same as the physical data. As described above, the present invention is able to detect the timing of the overflow and solve the overflow problem.

[0022] As described above, the present invention includes the following advantages:

1. When the clock frequency of the transmitter is different from the receiver, the present invention is able to detect the timing of the underflow and the overflow.

2. When the underflow or the overflow happens, the present invention is able to compensate properly, so that the bit number of the data received by the receiver is the same as the physical data. Thus, the underflow and the overflow problems can be solved.

[0023] Although the invention has been described with reference to a particular embodiment thereof, it will be apparent to one of the ordinary skill in the art that modifications to the described embodiment may be made without departing from the spirit of the invention. Accordingly, the scope of the invention will be defined by the attached claims not by the above detailed description.